

03/01/02 1132 U.S. PTO

11046 U.S. PTO
10/085009
03/01/02

Docket No.: 60188-156

UTILITY PATENT APPLICATION
UNDER 37 CFR 1.53(b)

Box PATENT APPLICATION
Commissioner for Patents
Washington, DC 20231
Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Masahiro FUKUI, Naoki HAYASHI
FOR: WIRING METHOD IN LAYOUT DESIGN OF SEMICONDUCTOR
INTEGRATED CIRCUIT, SEMICONDUCTOR INTEGRATED CIRCUIT AND
FUNCTIONAL MACRO

Enclosed are:

- ☒ 66 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☒ Certified copy of Japanese Patent Application No. 2001-063491
- ☒ 13 sheets of formal drawing.
- ☒ An assignment of the invention to Matsushita Electric Industrial Co., Ltd.
and the assignment recordation fee.
- ☒ An associate power of attorney.
- ☒ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard
- ☒ Preliminary Amendment

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	40	-20	20	\$18.00	\$360.00
Independent Claims	10	-3	7	\$84.00	\$588.00
Multiple Dependent Claim(s)					\$0.00
Basic Fee					\$740.00
Total of Above Calculations					\$1,688.00
Less 1/2 for Small Entity					\$0.00
Assignment & Recording Fee					\$40.00
Total Fee					\$1,728.00



20277

PATENT TRADEMARK OFFICE

2001-063491

[illegible]